R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments may be found in the specification, for example, on page 5 lines 11-13, page 7 lines 4-8, page 5 lines 12-15, page 9 lines 4-7, page 11 lines 1-19 and FIGS. 1, 2, 4 and 5, as originally filed. Thus, no new matter has been added.

OBJECTION TO THE SPECIFICATION

The objection to the title of the invention for not being descriptive is respectfully traversed and should be withdrawn.

Independent claim 1 provides a register stack. Independent claim 10 provides a method of controlling a register stack. Independent claim 15 provides a register stack means. Therefore, the title "Configurable Hardware Register Stack for CPU Architectures" appears to be descriptive. As such, the Examiner is respectfully requested to either (i) suggest a new title or (ii) withdraw the objection.

OBJECTION TO THE DRAWINGS

The objection to the drawings is respectfully traversed and should be withdrawn. A PTO-948 form has not been provided with

the Office Action to indicate what informalities should be corrected. Furthermore, the form paragraph 6.21 (see MPEP §608.02(b)) reproduced in the Office Action fails to identify what defect has been discovered in the content of the drawings. Therefore, the Examiner is respectfully requested to either (i) provide a PTO-948 form identifying the informalities, (ii) identify the detects discovered in the contents of the drawings or (iii) withdraw the objection.

CLAIM REJECTIONS UNDER 35 U.S.C. §112

The rejection of claim 15 under 35 U.S.C. §112, first paragraph enablement, has been obviated by appropriate amendment and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-3, 5-11 and 13-20 under 35 U.S.C. §102(b) as being anticipated by Watson '132 has been obviated in part, is respectfully traversed in part, and should be withdrawn.

Watson concerns register file with multi-tasking support (Title).

Claim 1 provides a structure comprising a register stack, a controller and a state register. Watson only appears to discuss a register file 23 (asserted similar to the claimed register stack), an index modifier 35, a loop register, an instruction execution unit 21, a program memory 29 an ALU 25, a streamer

register 33 and a data memory 27. However, none of the index modifier 35, the instruction execution unit 21 or ALU 25 appear to have all of the limitations of the claimed controller. None of the looper register, the program memory 29, the streamer register 33 or the data memory 27 appear to store data similar to the claimed register states. Therefore, Watson does not appear to disclose or suggest a structure comprising a register stack, a controller and a state register as presently claimed.

Claim 1 further provides that the controller is configured to store a plurality of register states, wherein each of the register states has one associated register of the registers (in the register stack). Despite the assertion in the Office Action, column 12 lines 32-45 of Watson appear to be silent regarding both a controller and storage of register states each associated with one of the registers in the register stack:

> FIGS. 9 and 10 illustrate a further register file addressing particularly suited for user and supervisor local addressing. If the address space 90 indicates global registers 94, then the lower 32 global registers 94 may be addressed. However, if the address space 90 indicates local registers 95, then a mode bit 91 (in a status register) will be used to determine whether it is intended for a user local or a supervisor local register. Then, the local register, whether it is supervisor or user, can be accessed based on the relative address within the local portion of the address space 90. Note that both the user and supervisor registers have their respective RFBU 96 (Register File Base User) and RFBS 97 (Register File Base Supervisor) for accessing the target register based on the relative address.

The "local state" and "user state" argued in the Office Action do not appear to be associated with one of the registers in the register file 23 of Watson (asserted similar to the claimed

register stack). Therefore, Watson does not appear to disclose or suggest that the controller is configured to store a plurality of register states, wherein each of the register states has one associated register of the registers as presently claimed.

Claim 1 further provides a state register connected to the control circuit and configured to present the register states to the control circuit. In contrast, Watson appears to be silent regarding a status register (asserted to store the claimed register states) being connected to some unidentified control circuit. Therefore, Watson does not appear to disclose or suggest a state register connected to the control circuit and configured to present the register states to the control circuit as presently claimed. Claim 15 provides language similar to claim 1. As such, claims 1 and 15 are fully patentable over the cited reference and the rejection should be withdrawn.

Claim 10 provides a step for comparing a register address with a plurality of register states to present a gating signal. Despite the assertion in the Office Action, the text in column 12 32-45 of Watson appears to be silent regarding a comparison operation between a register address and register states:

> FIGS. 9 and 10 illustrate a further register file addressing particularly suited for user and supervisor local addressing. If the address space 90 indicates global registers 94, then the lower 32 global registers 94 may be addressed. However, if the address space 90 indicates local registers 95, then a mode bit 91 (in a status register) will be used to determine whether it is intended for a user local or a supervisor local register. Then, the local register, whether it is supervisor or user, can be accessed based on the relative address within the local portion of the address space 90. Note that both the user and supervisor registers have their respective RFBU 96

(Register File Base User) and RFBS 97 (Register File Base Supervisor) for accessing the target register based on the relative address.

Nowhere in the above text, or in any other section does Watson appear to expressly or inherently discuss comparing register states with a register address. Furthermore, the following statements made in the Office Action do not appear to be mentioned in the above reproduced text or any other text of Watson:

> [N]ote that the relative offset is compared to see if it corresponds to a global register, a local user register, or a local supervisor register.
>
> Once it is determined what type of register is to be accessed, the corresponding base address is sent to the adder (for adding to the relative offset - see column 7, line 4, for instance)...
>
> [A] gating signal would inherently tell the adder to proceed with adding.
>
> This signal is a gating signal because it controls the accessing of the adder input signals (base and offset).

Therefore, the Examiner is respectfully requested to either (i) identify where Watson expressly or inherently discloses the above statements or (ii) withdraw the rejection.

Furthermore, Applicant's representative respectfully traverses the assertion in the Office Action that a gating signal would inherently tell an adder to proceed with adding. Inherency requires certainty of results, not mere possibility.[1] In contrast, adders that operate continuously on the input data are well known in the art. In another example, Watson appears to disclose in

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[1] See, e.g., *Ethyl Molded Products Co. v. Betts Package, Inc.*, 9 U.S.P.Q. 2d 1001 (E.D.Ky 1988). See also, In re Oelrich, 666 F.2d 578, 581, 212 USPQ 323, 326 (C.C.P.A. 1981).

column 7 line 4 an adder model that does not involve a gating signal. Therefore, a gating signal input to an adder is not a certainty and thus not inherent.

Claim 10 further provides a step for gating a segment count with the gating signal to present a segment address. Despite the assertion in the Office Action, the text in column 7, line 4 of Watson appears to be silent regarding both a segment count, a gating signal and a segment address:

a=i+REG

Watson further states in column 7, lines 1-3 that "i" is a relative address from an instruction field, "REG" is a global base address, "a" is an absolute address and the "+" is an addition operation, not a gating operation. Therefore, Watson does not appear to disclose or suggest a step for gating a segment count with the gating signal to present a segment address as presently claimed.

Claim 10 further provides a step for addressing a plurality of segments within the register stack with the segment address. In contrast, column 5, lines 59-63 of Watson appear to contemplate that the register file 23 (asserted similar to the claimed register stack) is addressed only through an absolute address. Watson appears to be silent regarding a segment address. Therefore, Watson does not appear to disclose or suggest a step for addressing a plurality of segments within the register stack with the segment address as presently claimed. As such, claim 10 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 3 provides that at least one of the register states is fixed in a stackable state indicating that data can be pushed onto the one associated register. In contrast, Watson appears to be silent regarding any of the registers within the register file 23 (asserted similar to the claimed register stack) being **fixed** as stackable. Furthermore, column 2, line 66 thru column 3, line 6 of Watson appears to contemplate that the registers can be designated differently at different times. None of the registers in the register file 23 of Watson to appear to have a fixed state. Therefore, Watson does not appear to disclose or suggest that at least one of the register states is fixed in a stackable state indicating that data can be pushed onto the one associated register as presently claimed. As such, claim 3 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 2 provides at least one of the register states is fixed in a global state indicating that data cannot be pushed onto the one associated register. In contrast, Watson appears to be silent regarding (i) register within the register file 23 having a fixed state (see argument above for claim 3) and (ii) being unable to push or pop data to/from a global register. Therefore, Watson does not appear to disclose or suggest at least one of the register states is fixed in a global state indicating that data cannot be pushed onto the one associated register as presently claimed. As such, claim 2 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 6 provides that the status circuit comprises a comparator configured to present the gating signal by comparing the register states and the register address signal. In contrast, Watson appears to be silent regarding a comparator within a status circuit. Furthermore, Applicant's representative respectfully traverses the assertion in the Office Action that comparing is inherent to knowing a bit in a register. In particular, a bit in a register can be determined by reading the content of the register. A comparing operation is not a certainty and thus is not inherent. Therefore, Watson does not appear to disclose or suggest that the status circuit comprises a comparator configured to present the gating signal by comparing the register states and the register address signal as presently claimed. As such, claim 6 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 11 provides a step for presenting a signal communicating the plurality of register states. In contrast, Watson appears to be silent regarding a signal that communicates all of the global, local user and local supervisor states (asserted similar to the claimed register states). Furthermore, Applicant's representative respectfully traverses the assertion in the Office Action that a signal communicating all of the states in inherent. In particular, each state may be communicated thru individual signals, one at a time. A signal communicating a plurality of states is not certain and thus is not inherent. Therefore, Watson does not appear to disclose or suggest a step for presenting a

signal communicating the plurality of register states as presently claimed. As such, claim 11 is fully patentable over the cited reference and the rejection should be withdrawn.

Claims 5, 7-9 and 13-20 depend from claims 1 and 10, which are now believed to be allowable. Since the dependent claims include all of the limitations of the independent claims, claims 5, 7-9 and 13-20 are fully patentable over the cited references and the rejections should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claim 4 under 35 U.S.C. §103(a) as being unpatentable over Watson in view of Guttag '042 is respectfully traversed and should be withdrawn.

The rejection of claim 12 under 35 U.S.C. §103(a) as being unpatentable over Watson in view of Official has been obviated by appropriate amendment and should be withdrawn.

Watson concerns register file with multi-tasking support (Title). Guttag concerns a microprocessor system with instruction pre-fetch (Title).

Regarding claim 4, the teachings of Guttag appear to conflict with the well known benefit to have the register on-chip, as asserted in the Office Action. In particular, Guttag states in column 4, line 64 thru column 5, line 3 that having the registers external to the processor "allows faster response to interrupts and increased programming flexibility, compared to the traditional method of having most operands and return addresses stored in

registers on the chip 1." Assuming Guttag is correct, one of ordinary skill in the art would appear to be motivated NOT to keep any of the stack registers on the same chip as the processor as is taught by Watson. The proposed combination appears to slow down the overall response time to interrupts. On the other hand, if the Office Action is correct that on-chip registers are accessed quicker than off-chip registers, one of ordinary skill in the art would appear NOT to be motivated to implement any registers off-chip as taught by Guttag. The proposed combination appears to slow down the overall operation of the processor. Therefore, the proposed modification appears to incorporate the disadvantages of both Guttag and the well known on-chip architecture. Given that the above disadvantages appear to offset any perceived benefit, there appears to be no clear and particular motivation for one of ordinary skill in the art to make the combination proposed in the Office Action. As such, *prima facie* obviousness has not been established and the rejection of claim 4 should be withdrawn.

Claim 12 provides a step for writing the plurality of register states into a register under software control in response to a reset handler operation for a processor executing the software. In contrast, both Watson and the Official Notice appear to be silent regarding software controlling what is written for the register states in response to a reset handler operation. Therefore, Watson and the Official Notice, alone or in combination, do not appear to teach or suggest a step for writing the plurality of register states into a register under software control in

response to a reset handler operation for a processor executing the software as presently claimed.

Furthermore, no clear and particular evidence of motivation to modify Watson has been established. The fact that references can be combined or modified is not sufficient to establish *prima facie* obviousness (MPEP §2143.01). Therefore, the Examiner is respectfully requested to either (i) provide evidence why one of ordinary skill in the art would make the proposed modification or (ii) withdraw the rejection of claim 12.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicant's representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

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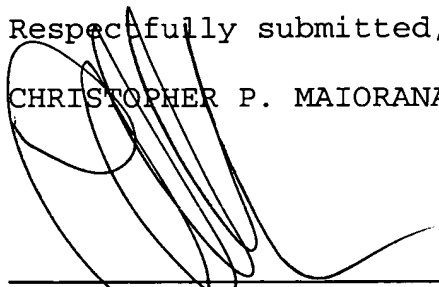

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